

Ayden Logan

Senior Staff ESD Engineer

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📍 Phoenix, AZ 85004

STRENGTHS

- ♥ **Risk Based Reviews**
Risk reviews turned uncertain protection behavior into clear choices, and design teams gained confidence before sign off.
- 🔍 **Silicon Debug**
Failure investigations began with careful evidence. That habit helped teams separate device behavior from layout assumptions.
- 🌐 **Global Collaboration**
Global reviewers often needed a concise technical story, so findings were shaped for teams across Japan and Asia.
- 📖 **Library Qualification**
Reusable libraries became easier to trust after characterization results, verification checks, and design guidance stayed connected.
- ✍ **Technical Writing**
Clear reports gave customers and engineers a shared reference when qualification decisions carried product risk.

SKILLS

ESD Latch Up High Voltage BCD
HBM CDM TLP Analog ICs
Power Management
Mixed Signal ICs
ESD Device Physics
Isolation Techniques
Reliability Analysis
Silicon Characterization
Failure Analysis Technical Writing

SUMMARY

Senior Staff ESD Engineer with 10 years of semiconductor experience across **High Voltage BCD**, analog, **power management**, and **mixed signal ICs**. Leads ESD and Latch Up design reviews, protection structure development, library qualification, risk assessment, and design sign off for automotive and industrial products. Applies **ESD device physics**, isolation techniques, HBM, CDM, TLP, silicon characterization, reliability analysis, and failure analysis to solve difficult product issues. Works closely with foundries, technology development teams, product designers, customers, and engineering groups in Japan and Asia. Uses Cadence analog IC development flows and Calibre PERC verification to connect device behavior with layout decisions. Clear technical writing and practical IEC EMC awareness support sound decisions, dependable qualification, and productive global collaboration.

EXPERIENCE

Senior Staff ESD Engineer

Solstice Microdevices 📅 January 2023 - Present 📍 Phoenix, AZ

Leads ESD and **Latch Up** engineering for High Voltage BCD analog, power, and mixed signal products. Owns protection architecture, design reviews, qualification planning, silicon debug, library release, risk assessment, and sign off. Connects internal designers, foundries, customers, and global engineering reviewers through clear technical evidence.

- Led **High Voltage BCD** reviews, resolving isolation risks before analog product sign off
- Designed protection structures for power domains and sensitive interfaces, preserving reliable current paths
- Directed **HBM**, **CDM**, and TLP characterization, turning lab evidence into design guidance
- Traced silicon failures through electrical data and physical evidence, clarifying corrective actions
- Qualified reusable **ESD libraries** through Cadence flows and **Calibre PERC** checks before adoption
- Presented product risk assessments to designers, foundries, customers, and global reviewers

Principal ESD Design Engineer

Mesa Analog Semiconductor 📅 June 2020 - December 2022 📍 Tempe, AZ

Owned ESD device development for power management and mixed signal products using High Voltage BCD processes. Guided clamp evaluation, technology reviews, design rule authorship, failure investigations, and collaboration with process teams. Supported **system level ESD** discussions when IEC EMC stress affected device protection choices.

- Developed **High Voltage BCD** protection devices for **power management** and mixed signal products
- Evaluated clamp triggers and current paths through **TLP** characterization, exposing isolation interactions
- Authored design rules and review checklists linking device physics with **reliability** constraints
- Partnered with process teams during technology changes, updating qualified protection options
- Investigated silicon failures, documenting root causes, corrective actions, and residual product risk
- Supported **IEC EMC** discussions where system stress shaped device level protection strategy

Senior ESD Engineer

Copper Ridge Integrated Circuits 📅 July 2018 - May 2020 📍 Chandler, AZ

Owned ESD verification for analog and power IC programs from schematic review through silicon characterization. Managed protection requirements, verification planning, lab result interpretation, designer resolution, technical reporting, and customer discussion support. Balanced parasitics, leakage, area, high voltage operation, and qualification targets.

- Owned **ESD** verification from schematic review through **silicon characterization** for analog programs
- Applied HBM and CDM requirements across pad structures, power clamps, and internal paths

LANGUAGES

English	Native
Japanese	Beginner

MY CAREER



- Senior Staff ESD Engineer at Solstice Microdevices (3.7 Years)
- Principal ESD Design Engineer at Mesa Analog Semiconductor (2.5 Years)
- Senior ESD Engineer at Copper Ridge Integrated Circuits (1.8 Years)
- ESD Design Engineer at Desert Peak Semiconductors (2 Years)

- Used Cadence and **Calibre PERC** to identify protection rule issues before tapeout
- Built characterization plans, comparing laboratory results with qualification targets and failure signatures
- Resolved parasitic and leakage conflicts with designers during high voltage layout reviews
- Produced technical reports supporting **design reviews**, qualification decisions, and customer discussions

ESD Design Engineer

Desert Peak Semiconductors 📅 June 2016 - June 2018 📍 Scottsdale, AZ

Supported device design and characterization for analog and mixed signal products under senior engineering review. Executed HBM, CDM, and TLP plans, organized silicon evidence, prepared Cadence review data, and contributed failure analysis for technology development and design teams.

- Supported **ESD** device design and characterization for analog and mixed signal products
- Executed HBM, CDM, and TLP plans under senior engineering review and organized findings
- Analyzed protection paths and isolation structures using device physics fundamentals
- Prepared Cadence review data and applied rule based verification before tapeout
- Contributed **failure analysis** evidence during reviews of damaged protection structures
- Documented characterization methods and findings for design and **technology development teams**

PROJECTS

High Voltage BCD Library Qualification 📅 2024

Built a reusable qualification approach for ESD libraries, connecting Calibre PERC checks, silicon evidence, and design review decisions. Shared findings with designers and global reviewers to support confident product adoption.

Mixed Signal Silicon Failure Analysis 📅 2022

Investigated protection failures across mixed signal silicon using electrical characterization, TLP evidence, and physical findings. Converted root cause conclusions into corrective actions and clearer product risk decisions.

LEADERSHIP & AWARDS

- Recognized by design leadership for dependable High Voltage BCD ESD sign off across complex product reviews.
- Selected as a trusted technical reviewer for silicon failure analysis and protection library qualification.
- Led cross regional technical discussions that connected engineering teams in Japan, Asia, and North America.

EDUCATION

Master of Science in Electrical Engineering

Arizona State University 🎓 GPA: 4.0 📅 2016 📍 Tempe, AZ

Coursework: ESD device physics, analog IC design, semiconductor reliability, electrical characterization

CERTIFICATIONS

- Cadence Analog IC Design Flow Continuing Education 📅 2024
- ESD Association Device Testing Fundamentals Training 📅 2022

TECHNICAL SKILLS

- **ESD Testing:** HBM, CDM, TLP
- **ESD Design:** Protection Structures, ESD Libraries, Device Limits
- **High Voltage Devices:** High Voltage BCD, Analog Devices, Power Devices
- **Reliability Engineering:** Latch Up, Reliability Analysis, Risk Assessment
- **Silicon Analysis:** Silicon Characterization, Silicon Debug, Failure Analysis

- **IC Design Tools:** Cadence, Calibre PERC, Analog IC Flow
- **Isolation Design:** Isolation Structures, Isolation Boundaries, Current Paths
- **IC Product Types:** Analog ICs, Power Management, Mixed Signal ICs
- **Design Governance:** Design Reviews, Design Guidelines, Design Sign Off
- **System ESD:** IEC EMC, System Level ESD, Electromagnetic Compatibility
- **Documentation:** Technical Writing, Technical Reports, Review Checklists
- **Engineering Collaboration:** Foundries, Technology Development, Customer Reviews

PROFESSIONAL AFFILIATIONS

- Active participant in semiconductor reliability and ESD engineering communities.
- Collaborates with foundry and technology development partners on protection methods and qualification evidence.

ADDITIONAL INFORMATION

Work Status : Authorized to work in United States. No sponsorship required.

REFERENCES

AVAILABLE ON REQUEST